ANALOG DEVICES

AN-378
APPLICATION NOTE

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Reducing the Average Power Consumption of Accelerometers

by Charles Kitchin, Mike Shuster and Bob Briano

The use of a simple power cycling circuit provides a dramatic reduction in the average current consumption of the ADXL50 and ADXL05 devices. In low bandwidth applications such as shipping recorders, a simple, low cost circuit can provide substantial power reduction. If a microprocessor is available, only the circuit of Figure 1 is needed; the microprocessor supplies a TTL clock pulse to gate buffer transistor Q2, which cycles the supply voltage on and off. Figures 2 through 4 show typical wave forms of the accelerometer being operated with a 10% duty cycle: 1 ms on, 9 ms off. This reduces the average current consumption of the accelerometer from 10 mA to 1 mA, providing a power reduction of 90%.

The lower trace of Figures 2 and 3 is the output voltage appearing at V_{PR} (Pin 8). The lower trace of Figure 4 is the buffer output (Pin 9) with the buffer operating at unity gain. A 0.01 µF capacitor was connected across the feedback resistor of the buffer to improve its transient characteristics. The optimum value for this capacitor will change with buffer gain and the cycling pulse rate. The µP should sample acceleration during the interval between the time the 0 *g* level has stabilized (approximately 400 µs using a 0.022 µF demod cap) and the end of the pulse duration. For the example shown in Figures 2 through 4, this is between 400 µs and 1 ms after Q2 receives a logic "low" from the µP.

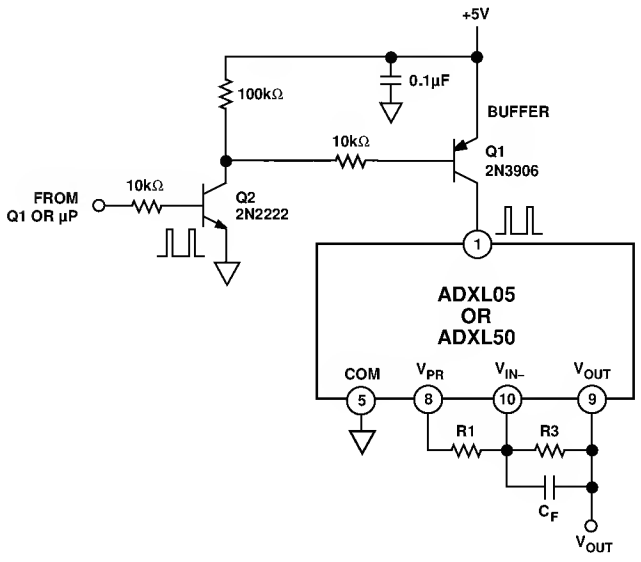

Figure 1. Basic Power Cycling Circuit

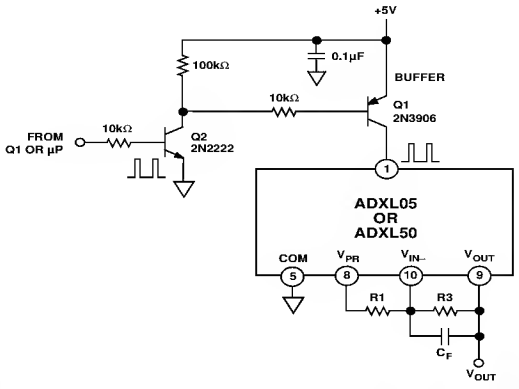

Figure 2. Top Trace: Voltage at Pin 1
Bottom Trace: Output at V_{PR}

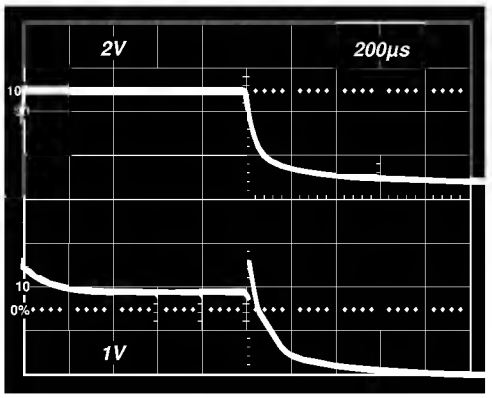

Figure 3. Top Trace: Voltage at Pin 1
Bottom Trace: Output at V_{PR}

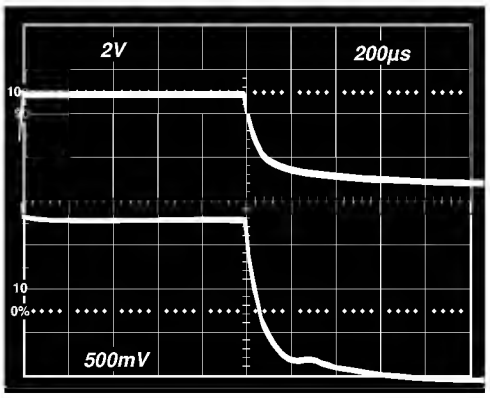

Figure 4. Top Trace: Voltage at Pin 1 Bottom Trace: Buffer Output with R1 = R3 = 100 kΩ, CF = 0.01 µF

The measurement bandwidth of a power-cycled circuit will be set by the clock pulse rate and duty cycle. In this example, 1 sample can be taken every 10 ms which is 100 samples per second or 100 Hz. As defined by the "Nyquist criteria," the best case measurement bandwidth is $F_S/2$ or half the clock frequency. Therefore, 50 Hz signals can be processed if adequate digital filtering is provided. Higher measurement bandwidths can be achieved by reducing the size of the demodulation capacitor below 0.022 µF and increasing the pulse frequency.

Figure 5 is a low cost timer circuit for applications not using a µP. The timer frequency can be changed by using different values for capacitors C1 and C2. The duty cycle is set by trim potentiometer R2b. Transistor Q1 inverts the output pulse of the 555 timer so that the duty cycle is correct when the pulse is reinverted again by buffer transistor, Q2. The timer/inverter circuit adds about 700 µA to the total supply current.

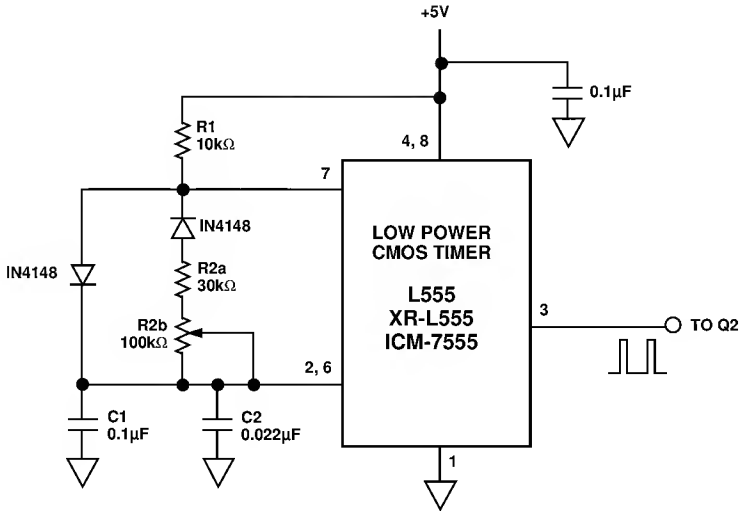

Figure 5. Timer/Inverter Circuit Duty Cycle Range 1:4 to 1:13

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